Claims

[c1] A converter circuit for converting a double width data bus transmitting data at a single rate to a single width data bus transmitting data at a double rate, the converter circuit comprising:

a first data bus and a second data bus respectively transporting first data characterized as even data represented by d0, d2, d4, d6, ... d_n and second data characterized as odd data represented by d1, d3, d5, d7, ... d_{n+1}, where n = 0, 2, ... , the even data and the odd data being emitted at a single rate;

a first clock generator for generating a first clock, characterized as a positive clock, and an inverted phase thereof, characterized as a negative clock;

a data mixer for mixing even data d_n and odd data d_{n+1} to generate two mixed data characterized as $d_n$mix and d_{n+1}mix respectively, wherein $d_n$mix is a result of multiplexing of d_n and inverted data NOT(d_n) by mixed data d_{n-1}mix on a rising edge of the positive clock and d_{n+1}mix is a result of multiplexing of d_{n+1} and inverted data NOT(d_{n+1}) by mixed data $d_n$mix on a rising edge of the negative clock;

an XOR circuit for performing an XOR function on mixed data $d_n$mix and d_{n+1}mix to generate first output data and for performing an XOR function on mixed data d_{n+1}mix and d_{n+2}mix to generate second output data, to enable

transmission of the first output data and the second output data on a single width data bus at a double rate; and

a second clock generator for generating a second clock synchronous with the first output data and the second output data.

[c2] A converter circuit according to claim 1, wherein said XOR circuit comprises three two-way NAND gates so that the XOR function is performed according to the relation:

$XOR(d_n mix, d_{n+1} mix) = NAND(NAND(d_n mix, d_{n+1} mixinv), NAND(d_n mixinv, d_{n+1} mix))$

wherein $d_n mixinv = NOT(d_n mix)$ and $d_{n+1} mixinv = NOT(d_{n+1} mix)$.

[c3] A converter circuit according to claim 1, wherein said data mixer further comprises:

a first data mixer latch having a clock input and a data input coupled to said first data bus to latch even data;

a first multiplexor coupled to said first data mixer latch, said first multiplexor having as data inputs an output of said first data mixer latch and the complement thereof, and having a control input characterized as a first control input;

a second data mixer latch having a clock input and a data input coupled to said first multiplexor to latch an output of said first multiplexor at a next clock cycle, the clock inputs of said first data mixer latch and said second data mixer latch being

configured to receive the positive clock;

a third data mixer latch having a clock input and a data input coupled to said second data bus to latch odd data;

a second multiplexor coupled to said third data mixer latch, said second multiplexor having as data inputs an output of said third data mixer latch and the complement thereof, and having a control input characterized as a second control input;

a fourth data mixer latch having a clock input and a data input coupled to said second multiplexor to latch an output of said second multiplexor at a next clock cycle, the clock inputs of said third data mixer latch and said fourth data mixer latch being configured to receive the negative clock;

wherein the first control input is connected to an output of said fourth data mixer latch and the second control input is connected to an output of said second data mixer latch,

so as to generate data $d_n$mix at the output of said second data mixer latch and data d_{n+1}mix at the output of said fourth data mixer latch.

[c4] A converter circuit according to claim 1, wherein said XOR circuit comprises:

a first inverter for generating the complement of data $d_n$mix characterized as $d_n$mixinv;

a second inverter for generating the complement of data d_{n+1}mix characterized as d_{n+1}mixinv;

a first XOR circuit latch having a clock input coupled to the positive clock and a data input given by $d_n$mix;

a second XOR circuit latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mixinv;

a first NAND gate connected to outputs of said first XOR circuit latch and said second XOR circuit latch respectively;

a third XOR circuit latch having a clock input coupled to the positive clock and a data input given by $d_n$mixinv;

a fourth XOR circuit latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mix;

a second NAND gate connected to outputs of said third XOR circuit latch and said fourth XOR circuit latch respectively; and

a third NAND gate connected to outputs of said first NAND gate and said second NAND gate respectively.

[c5] A converter circuit according to claim 2, wherein said XOR circuit comprises:

a first inverter for generating the complement of data $d_n$mix characterized as $d_n$mixinv;

a second inverter for generating the complement of data d_{n+1}mix characterized as d_{n+1}mixinv;

a first XOR circuit latch having a clock input coupled to the positive clock and a data input given by $d_n$mix;

a second XOR circuit latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mixinv;

a first NAND gate connected to outputs of said first XOR circuit latch and said second XOR circuit latch respectively;

a third XOR circuit latch having a clock input coupled to the positive clock and a data input given by $d_n$mixinv;

a fourth XOR circuit latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mix;

a second NAND gate connected to outputs of said third XOR circuit latch and said fourth XOR circuit latch respectively; and

a third NAND gate connected to outputs of said first NAND gate and said second NAND gate respectively.

[c6] A converter circuit for converting a double width data bus transmitting data at a single rate to a single width data bus transmitting data at a double rate, the converter circuit comprising:

a first data bus and a second data bus respectively transporting first data characterized as even data represented by d0, d2, d4, d6, ... d_n and second data characterized as odd data represented by d1, d3, d5, d7, ... d_{n+1}, where n = 0, 2, ... , the even data and the odd data being emitted at a single rate;

a clock generator for generating a first clock, characterized as a positive clock, and an inverted phase thereof, characterized as a negative clock;

a first data latch having a clock input and a data input coupled to said first data bus to latch even data;

a first multiplexor coupled to said first data latch, said first multiplexor having as data inputs an output of said first data latch and the complement thereof, and having a control input characterized as a first control input;

a second data latch having a clock input and a data input coupled to said first multiplexor to latch an output of said first multiplexor at a next clock cycle, the clock inputs of said first data latch and said second data latch being configured to receive the positive clock;

a third data latch having a clock input and a data input coupled to said second data bus to latch odd data;

a second multiplexor coupled to said third data latch, said second multiplexor having as data inputs an output of said third data latch and the complement thereof, and having a control input characterized as a second control input;

a fourth data latch having a clock input and a data input coupled to said second multiplexor to latch an output of said second multiplexor at a next clock cycle, the clock inputs of said third data latch and said fourth data latch being configured to receive the negative clock;

wherein the first control input is connected to an output of said fourth data latch and the second control input is connected to an output of said second data latch, so as to generate data $d_n$mix at the output of said second data latch and data d_{n+1}mix at the output of said fourth data latch;

a first inverter for generating the complement of data $d_n$mix characterized as $d_n$mixinv;

a second inverter for generating the complement of data d_{n+1}mix characterized as d_{n+1}mixinv;

a fifth data latch having a clock input coupled to the positive clock and a data input given by $d_n$mix;

a sixth data latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mixinv;

a first NAND gate connected to outputs of said fifth data latch and said sixth data latch respectively;

a seventh data latch having a clock input coupled to the positive clock and a data input given by $d_n$mixinv;

an eighth data latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mix;

a second NAND gate connected to outputs of said seventh data latch and said eighth data latch respectively; and

a third NAND gate connected to outputs of said first NAND gate and said second NAND gate.